IMPERIAL COLLEGE LONDON

Design Engineering MEng EXAMINATIONS 2016

For Internal Students of the Imperial College of Science, Technology and Medicine
This paper is also taken for the relevant examination for the Associateship or Diploma

Engineering Analysis EA 1.3 - Electronics

SAMPLE EXAMINATION PAPER

All questions in this sample paper are taken from the Tutorial Problem Sheets to illustrate the type of questions you may expect. Solutions are therefore all available from the Course Webpage.

This paper contains THIRTEEN questions.

Attempt ALL questions.

Write your answers in the ANSWER BOOKS provided.

The numbers of marks shown by each question are for your guidance only; they indicate approximately how the examiners intend to distribute the marks for this paper.

This is a CLOSED BOOK Examination.

Information for Candidates:

You may also put part of your answers in the answer book if you need more space. Make sure that your attach both the question paper and the answer book(s) together.

The following notation is used in this paper:

1. Unless explicitly indicated otherwise, all resistors are in kΩ and all currents are in mA.
2. Unless explicitly indicated otherwise, digital circuits are drawn with their inputs on the left and their outputs on the right.
3. Within a circuit, signals with the same name are connected together even if no connection is shown explicitly.
4. The notation X2:0 denotes the three-bit number X2, X1 and X0. The least significant bit of a binary number is always designated bit 0.
5. Signed binary numbers use 2's complement notation.

1. What single resistor is equivalent to the five-resistors sub-circuit shown in Figure 1?

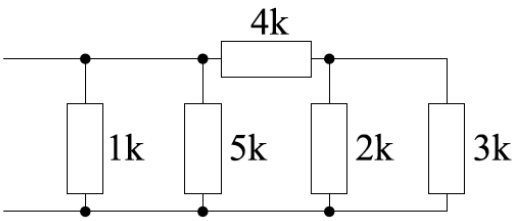

Figure 1

[4]

2. Calculate V_X in the circuit shown in Figure 2 using (a) nodal analysis and (b) superposition.

[4]

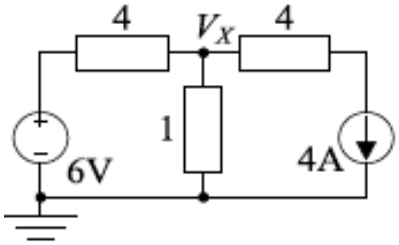

Figure 2

3. Calculate the Thevenin equivalent networks at the terminals A and B in Fig. 3 by combining resistors to simplify the circuit.

[4]

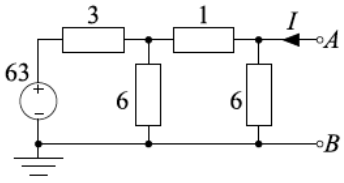

Figure 3

4. If $v(t) = \begin{cases} 0 & t < 0 \\ 5 & t \geq 0 \end{cases}$ in Fig. 4,

(a) Find an expression for $x(t)$ for $t \geq 0$.

[4]

(b) Sketch a graph of $x(t)$ for $-RC \leq t \leq 3RC$.

[4]

(c) Determine the time at which $x(t) = 4.5$.

[4]

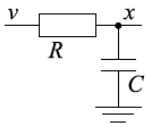

Figure 4

5. (a) For the following waveform 3 cos ωt + 4 sin ωt, determine its corresponding phasor in both complex form a+jb and in polar form.

[4]

(b) Calculate both the complex impedance and the complex admittance for the circuit shown in Figure 5.

[4]

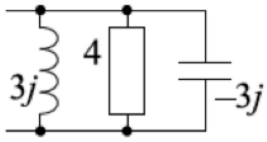

Figure 5

6. For the circuits in Fig. 6,

(a) Find the transfer function (i.e. frequency response) H(jω) = Y(jω)/X(jω).

[4]

(b) Find expressions for the low and high frequency asymptotes of H(jω).

[4]

(c) Sketch the straight line approximation to the magnitude response, |H(jω)|, indicating the frequency (in rad/s) and the gain of the approximation (in dB) at each of the corner frequencies.

[4]

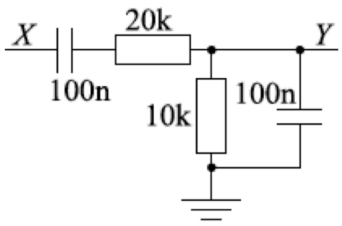

Figure 6

7. Find an expression for Y in the circuit shown in Figure 7 in terms of U_1 and U_2.

[8]

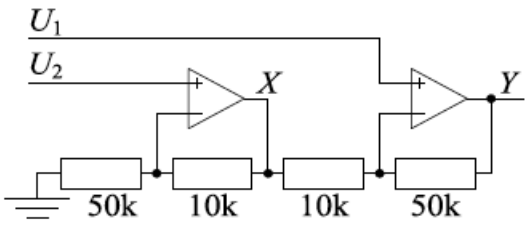

Figure 7

8. In the circuit diagram, the potentiometer resistance between the slider and ground is a x 40 kΩ

where $0 \le a \le 1$. Find the gain of the circuit, X/U as a function of a. What is the range of gains that the circuit can generate as a is varied.

[8]

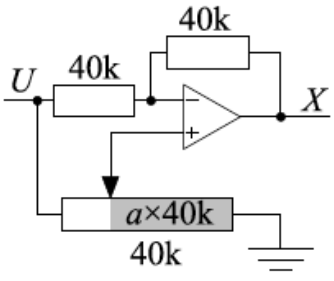

Figure 8

9. Convert the following numbers:

(a) Decimal number 1024 to binary.

[3]

(b) Decimal number 98 to hexadecimal.

[3]

(c) Binary 100000000 to hexadecimal and signed decimal.

[3]

(d) ASCII character 'U' to binary and hexadecimal.

[3]

10. In the circuit of Fig. 10, the output logic levels from the inverter are 0V and 5V and the inverter has a maximum output current of 2mA. The inverter senses a low voltage when its input is < 1.5 V. If x changes from logic 0 to logic 1, determine the delay until z changes. Ignore the inverter input currents and any delays inside the inverters themselves.

[8]

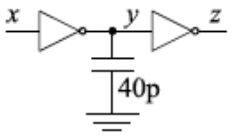

Figure 10

11. Show that the following circuit is equivalent to a single gate.

[8]

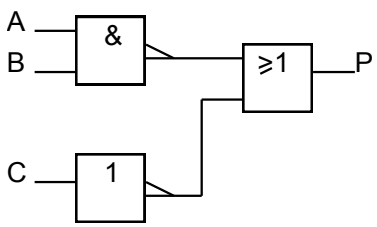

Figure 11 S6 Q17

12. Write out the truth table for the function S = A · B + C · D.

[4]

13. Using common sense and the rules of Boolean Algebra, simplify the following:

a) $\overline{(A + B)}.\overline{C}$

[4]

b) $A.(B + C) + C + \overline{A}.B.\overline{C}$

[4]

Solutions to the Sample Examination Paper

1. See Tutorial Problem Sheet 1 Question 8.

2. See Tutorial Problem Sheet 2 Question 3.

3. See Tutorial Problem Sheet 3 Question 3.

4. See Tutorial Problem Sheet 3 Question 14.

5. a) See Tutorial Problem Sheet 4 Question 1b.
   b) See Tutorial Problem Sheet 4 Question 5c.

6. See Tutorial Problem Sheet 4 Question 9.

7. See Tutorial Problem Sheet 5 Question 6.

8. See Tutorial Problem Sheet 5 Question 7.

9. a) See Tutorial Problem Sheet 6 Question 4c.
   b) See Tutorial Problem Sheet 6 Question 6b.
   c) See Tutorial Problem Sheet 6 Question 5b.
   d) See Tutorial Problem Sheet 6 Question 9.

10. See Tutorial Problem Sheet 3 Question 11.

11. See Tutorial Problem Sheet 6 Question 17.

12. See Tutorial Problem Sheet 6 Question 11.

13. See Tutorial Problem Sheet 6 Question 13 a & b.

